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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,143	08/20/2003	Vikram Magoon	P16184	7155

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EXAMINER	
VAN ROY, TOD THOMAS	

ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,143	MAGOON, VIKRAM	
	Examiner	Art Unit	
	Tod T. Van Roy	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The examiner acknowledges the amended specification, and withdraws the previous rejection to the figure.

Response to Arguments

Applicant's arguments filed 09/28/2005 have been fully considered but they are not persuasive.

The following is a brief summary of the applicant's arguments with the examiner's rebuttal to follow.

With regards to independent claims 1, 7, and 12, as well as their dependent claims.

1. *Kobayashi teaches away from a duty cycle control circuit by teaching a compensation circuit.*

The examiner agrees that Kobayashi teaches control circuit (#150) to act as a compensator to the duty cycle, but this circuit exerts control over the duty cycle being produced. In col.6-7 lines 53-35, Kobayashi teaches the function of the control circuit is to compensate (i.e., offset an error, neutralize an effect, or provide a means of counteracting variation – Merriam-Webster's Collegiate Dictionary, 10th edition, 1999) for the DC offset produced by circuits 102' and 104', thereby exerting a degree of control over the duty cycle (col.6 lines 60-64). As the control circuit has been shown to control the duty cycle, the limitations of the claims have been met.

2. *The incorporation of Larson with Kobayashi would render Kobayashi unsatisfactory, and would cease to function as intended.*

The examiner does not agree that the combination of Larson with Kobayashi would render Kobayashi unsatisfactory. Larson teaches the use of an average voltage signal effectively approximating the average power that enables prevention of pulse-to-pulse voltage variations (col.6 lines 24-27), influencing the voltage to the transistors Q1 and Q2, which would further improve compensations made to the duty cycle by the control circuit of Kobayashi, which influences transistors Q4 and Q24 (col.7 lines 8-12). It does not appear evident, by the disclosures of Larson or Kobayashi, or in the applicant's remarks, that the combination of the control circuit of Kobayashi and the average voltage signal effectively approximating the average power would render Kobayashi unsatisfactory, or cause it to cease its function.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-3, and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi (US 6373346) in view of Larson (US 5767704).

With respect to claims 1 and 7, Kobayashi teaches a laser driver circuit comprising an input stage (fig.6 #102,104) to receive an input signal (fig.6 IN+,IN-), a limiting amplifier (fig.6 #Q3, Q4 and #Q23, Q24 forming amps) to generate a pulse data output signal (figs. 3a-3b) comprising a duty cycle (seen in figs. 3a-3b), an output stage to modulate an output current signal based upon the pulse data output signal (fig.6 #108, col.5 lines 28-30), and a duty cycle control circuit (fig.6 #150) to control the duty cycle of the pulse data output signal. Kobayashi does not teach the duty cycle to be based on an average power of the pulse data output signal. Larson teaches a laser switching circuit using a capacitor to integrate a voltage signal effectively approximating the average power (col.6 lines 24-27). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver circuit of Kobayashi with the power averaging capacitor of Larson in order to stabilize the voltage (Larson, col.6 lines 30-32) and prevent voltage variations (Larson, col.6 lines 26-27) from affecting circuit performance.

With respect to claim 2, Kobayashi and Larson teach the laser driver as outlined in the rejection to claim 1, and further teach the input signal to comprise a bi-level signal (Kobayashi, fig.6 IN+, IN-; col.3 lines 47-48).

With respect to claims 3 and 8, Kobayashi and Larson teach the laser driver as outlined in the rejection to claim 1, and further teach the input stage to generate a differential signal on first and second terminals (fig.6 OUT+,OUT-) coupled to the limiting amplifier (fig.6, OUT+/- coupled to both limiting amps made up of #Q3/4 and #Q23/24), and wherein the duty cycle circuit comprises a current steering circuit to apply an offset current to al least one of the first and second terminals (col.6-7 lines 63-2) in response to the approximation of the average power of the pulse data output signal.

Claims 4-6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Larson and further in view of Gilliland et al. (US 6711189).

With respect to claims 4 and 9, Kobayashi and Larson teach the laser driver as outlined in the rejection to claim 1, and further teach a resistor pair, Rdcd1 and Rdcd2, located in the duty control circuit to be used to set the VDCD control voltage which effects the duty cycle of the pulse data output signal (Kobayashi, col.7 lines 2-11). Kobayashi and Larson do not teach the use of a potentiometer. Gilliland teaches a laser power control circuit in which a potentiometer is used to control an output voltage (abs. lines 4-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver duty control circuit with the potentiometer of Gilliland in order to allow for adjustability of the resistance values and hence the controlling voltage.

With respect to claims 5-6 and 10-11, Kobayashi, Larson, and Gilliland teach the laser driver as outlined in the rejection to claims 4 and 9 above, and further teach the duty control circuit to comprise a differential amplifier (Kobayashi, fig.6 formed from QDCD1 and QDCD2) to generate a differential voltage on first and second terminals (Kobayashi, col.7 lines 13-35, terminals leading to Q4 and Q24) in response to the pulse data output signal, and wherein the potentiometer (Kobayashi's Rdcd1 and Rdcd2 having been replaced by Gilliland's potentiometer) is coupled to the differential amplifier to determine a resistance between a voltage source (Kobayashi, fig.6 VDCD) and each of the first and second terminals (Kobayashi, col.7 lines 2-35, speaking of how the resistance changes the VDCD offset level applied through the two terminals to affect the output pulse data).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Larson and further in view of Kenny (US 6654565).

With respect to claim 12, Kobayashi and Larson teach the laser driver outlined in the rejection to claim 1, and further teach the driver to be used with a laser device (Kobayashi, col.1 lines 37-50). Kobayashi and Larson do not teach the laser driver to use a serializer. Kenny teaches a communication system utilizing a serializer (fig.9 #930). It would have been obvious at the time of the invention to combine the laser driver of Kobayashi and Larson with the serializer of Kenny in order to implement the laser and driver into a high-speed system (Kenny, col.19 lines 56-60).

Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Larson and Kenny, and further in view of Diaz et al. (US 6822987).

With respect to claim 13, Kobayashi, Larson, and Kenny teach the laser driving system as outlined in the rejection to claim 12, but do not teach the use of a SONET framer. Diaz teaches a high-speed laser array which uses a SONET framer (col.10 lines 46-48). It would have been obvious to one or ordinary skill in the art at the time of the invention to combine the laser driver system of Kobayashi, Larson and Kenny with the SONET framer of Diaz in order to provide for high bit rate during very high speed applications (Diaz, col.9 lines 50-57).

With respect to claims 14-17, Kobayashi, Larson, Kenny, and Diaz teach the laser system as outlined in the rejections to claims 12, and 13, while it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser system with a switch fabric coupled to the SONET, an Ethernet MAC and a multiplexed data bus since these components are well known and widely used in communications systems.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 12-17 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of copending Application No. 10/442829 in view of Kobayashi and Larson.

With respect to claim 12, Asuri teaches a serializer to provide a serial data signal in response to a parallel data signal, a laser device adapted to be coupled to an optical transmission medium to transmit an optical signal in the optical transmission medium, and a laser driver circuit (Asuri, claim 1). Asuri does not teach the specifics of the laser driver, i.e.: an input stage to receive an input signal, a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle', an output stage to modulate the current signal based upon the pulse data output signal', and a duty cycle adjustment circuit to adjust the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal. Kobayashi and Larson teach a laser driving circuit as outlined in the rejection to claim 1 above, which has these specific properties. It would have been obvious at the time of the invention to one of ordinary skill in the art to combine the laser system of Asuri with the laser driver of Kobayashi and Larson in order to allow for finer control of the output signal, namely taking a differential input signal and outputting a modulated differential signal (Kobayashi, abs. lines 2-5).

With respect to claims 13-17, Asuri, Kobayashi, and Larson teach the laser system outlined in the double patenting rejection to claim 12, and further teach the SONET framer to provide the parallel data signal (Asuri, claim 2), a switch fabric to be coupled to the SONET framer (Asuri, claim 3), an Ethernet MAC to provide the parallel data signal at a media independent interface (Asuri, claim 4), a multiplexed data bus to be coupled to the Ethernet MAC (Asuri, claim 5), and a switch fabric to again be coupled to the Ethernet MAC (Asuri, claim 6).

This is a provisional obviousness-type double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVR